

WHAT IS CLAIMED IS:

- 1 1. A semiconductor device comprising:  
2 a dielectric layer;  
3 a conductive line underlying the dielectric layer;  
4 a via formed in the dielectric layer and extending into the conductive line to form a via  
5 recess in the conductive line, the via recess formed in the conductive line having a depth of at  
6 least about 100 angstroms; and  
7 via-fill material filling the via recess and at least partially filling the via, such that the  
8 via-fill material is electrically connected to the conductive line.
- 1 2. The semiconductor device of claim 1, wherein the via-fill material comprises:  
2 a barrier layer at least partially lining interior surfaces of the via recess and at least  
3 partially lining interior surfaces of the via; and  
4 a conducting material, wherein the barrier layer is located between at least part of the  
5 conducting material and at least part of the dielectric layer.
- 1 3. The semiconductor device of claim 2, wherein the conducting material is electrically  
2 connected to the conductive line through the barrier layer.
- 1 4. The semiconductor device of claim 2, wherein the barrier layer comprises a material  
2 selected from a group consisting of tantalum, tantalum nitride, tungsten, compounds thereof,  
3 composites thereof, and combinations thereof.

1 5. The semiconductor device of claim 2, wherein the conducting material comprises  
2 material selected from a group consisting of metal alloy, copper, copper alloy, aluminum,  
3 aluminum alloy, tungsten, poly-crystalline silicon, compounds thereof, composites thereof, and  
4 combinations thereof.

1 6. The semiconductor device of claim 5, wherein the depth of the via recess formed in the  
2 conductive line is between about 150 angstroms and about 300 angstroms.

1 7. The semiconductor device of claim 1, wherein the dielectric layer comprises:  
2 a capped layer; and  
3 a layer of insulating material overlying the capped layer.

1 8. The semiconductor device of claim 7, wherein the capped layer is a material comprising  
2 silicon-carbon having a thickness less than about 600 angstroms.

1 9. The semiconductor device of claim 8, wherein the capped layer has at least 30% carbon.

1 10. The semiconductor device of claim 7, wherein the capped layer comprises carbon-doped  
2 silicon nitride ( $\text{Si}_x\text{N}_y\text{C}_z$ ).

1 11. The semiconductor device of claim 7, wherein the capped layer has a dielectric constant  
2 less than about 4.0.

1 12. The semiconductor device of claim 7, wherein the capped layer has a thickness of less  
2 than about 600 angstroms.

1 13. The semiconductor device of claim 7, wherein the insulating material has a dielectric  
2 constant less than about 3.

1 14. The semiconductor device of claim 7, wherein the insulating material comprises a  
2 material selected from a group consisting of SiO<sub>x</sub>C<sub>y</sub>, FSG, Spin-On-Glass, Spin-On-Polymers,  
3 and combinations thereof.

1 15. The semiconductor device of claim 7, wherein the size of the via is less than about 900  
2 angstroms.

1 16. The semiconductor device of claim 1, wherein the depth of the via recess formed in the  
2 conductive line is between about 150 angstroms and about 300 angstroms.

1 17. The semiconductor device of claim 1, wherein the depth of the via recess formed in the  
2 conductive line is between about 300 angstroms and about 600 angstroms.

1 18. The semiconductor device of claim 1, wherein the conductive line comprises a material  
2 selected from a group consisting of metal alloy, copper, aluminum, copper alloy, poly-crystalline  
3 silicon, metal silicide, compounds thereof, composites thereof, and combinations thereof.

1 19. The semiconductor device of claim 1, wherein the dielectric layer has a dual damascene  
2 structure comprising another conductive line formed therein and being electrically connected to  
3 the conducting material in the via.

1    20.    A semiconductor device comprising:  
2            a dielectric layer comprising an insulating material layer and a capped layer, and the  
3 capped layer having a dielectric constant less than about 4;  
4            a conductive line underlying the dielectric layer;  
5            a via formed in the insulating material layer, through the capped layer, and extending into  
6 the conductive line to form a via recess in the conductive line, the via recess formed in the  
7 conductive line having a depth of in a range from about 100 angstroms to about 600 angstroms;  
8 and  
9            via-fill material filling the via recess and at least partially filling the via, such that the  
10 via-fill material is electrically connected to the conductive line.

1    21.    The semiconductor device of claim 20, wherein the conductive line is substantially made  
2 of copper.

1    22.    The semiconductor device of claim 20, wherein the capped layer is made of material  
2 comprising silicon carbon and is located between the insulating material layer and the conductive  
3 line.

1    23.    A semiconductor device comprising:  
2            a dielectric layer comprising an insulating material layer and a capped layer, and the  
3 capped layer comprising silicon and carbon;  
4            a copper-based conductive line underlying the dielectric layer;  
5            a via formed in the insulating material layer, through the capped layer, and extending into  
6 the conductive line to form a via recess in the conductive line, the via recess formed in the  
7 conductive line having a depth of in a range from about 100 angstroms to about 600 angstroms;  
8 and  
9            via-fill material filling the via recess and at least partially filling the via, such that the  
10 via-fill material is electrically connected to the conductive line.

1    24.    The semiconductor device of claim 23, wherein the capped layer comprises at least 30%  
2 carbon.

1    25.    The semiconductor device of claim 23, wherein the size of the via is less than about 900  
2 angstroms.

1    26.    The semiconductor device of claim 23, wherein the depth of the via recess formed in the  
2 conductive line is between about 150 angstroms and 300 angstroms.

1    27.    The semiconductor device of claim 23, wherein the depth of the via recess formed in the  
2 conductive line is between about 300 angstroms and 600 angstroms.

1 28. A method of fabricating a semiconductor device comprising:  
2 forming a via in a dielectric layer and opening to a conductive line underlying the  
3 dielectric layer; and  
4 forming a via recess in the conductive line at the via, the via recess in the conductive line  
5 having a depth ranging from about 100 angstroms to about 600 angstroms.

1 29. The method of claim 28, wherein the conductive line is substantially made of copper.

1 30. The method of claim 28, further comprising:  
2 filling the via recess and at least partially filling the via with a via-fill material.

1 31. The method of claim 28, wherein the via-fill material comprises:  
2 a barrier layer at least partially lining interior surfaces of the via recess and at least  
3 partially lining interior surfaces of the via; and  
4 a conducting material, wherein the barrier layer is located between at least part of the  
5 conducting material and at least part of the dielectric layer.

1 32. The method of claim 28, wherein the dielectric layer comprises:  
2 a capped layer; and  
3 a layer of insulating material overlying the capped layer.

1 33. The method of claim 28, wherein the size of the via is less than about 900 angstroms.

1 34. The method of claim 28, wherein the forming of the via recess includes a pre-metal  
2 cleaning process performed after the forming of the via.

1 35. The method of claim 34, wherein the pre-metal cleaning is a process selected from a  
2 group consisting of an argon sputter, an ammonia-based reactive process, a hydrogen-based  
3 reactive process, and combinations thereof.